JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

Vision and Mission of the University

Vision

The University is primarily promoting quality of education in the areas of Science, Technology, Engineering and Mathematics (STEM) as four academic pillars of education, to excel in teaching, learning, research, consultancy and placements through innovative practices with global perspective.

Mission

1. Design an Industry relevant curriculum from time to time with a Global perspective
2. Promoting quality education by embracing ICT delivery mechanism with continuous pedagogy through e-learning mechanism
3. Spread across for industry collaborations with a focus to pre-training and placements for technology transfer to society
4. Establishing centers of excellence to promote research and innovations in multidisciplinary areas to bring in patent culture and consultancy practices
5. International Collaborations for student outreach
6. Facilitating international students to study in JNTUK to infuse cross culture learning practices.

Vision and Mission of the Institute

Vision and Mission of the Department

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Program Educational Objectives (PEOs)

PEO-1: Engage in critical thinking, research, and innovation to address real-world engineering problems, particularly in VLSI design and development.

PEO-2: Attain professional competence in solving complex problems across domains of analog, digital, RF, and mixed-signal VLSI subsystems, with proficiency in using industry-standard EDA tools.

PEO-3: Pursue lifelong learning as a means of enhancing knowledge base and skills necessary to contribute to the improvement of their profession and community.

Programme Outcomes

PO1: An ability to independently carry out research /investigation and development work to solve practical problems

PO2: An ability to write and present a substantial technical report/document

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

PO-4: Model and offer solutions to issues related to device, IC design, testing and EDA tool development

PO-5: Comprehend the state-of-the-art VLSI technologies

PO-6 : Characterize and design analog, digital, RF and mixed signal subsystems meeting given constraints under deep sub-micron environment

Mapping of PEOs with Pos:

	PO1	PO2	PO3	PO4	PO5	PO6
PEO1	H	M	H	H	M	M
PEO2	M	L	H	H	H	H
PEO3	L	M	M	L	M	M

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M.TECH

(VLSI, VLSI DESIGN, VLSI SYSTEM DESIGN, VLSI & MICRO-ELECTRONICS PROGRAMME)

Programme Course Structure & Syllabus

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Programme Structure R25 MTech (VLSI, VLSI Design, VLSI System Design, VLSI Micro-Electronic Programme)

I – Semester

S. No.	Course Code	Course Title	L	T	P	C
1	PC	Digital CMOS Circuit Design	3	1	0	4
2	PC	Analog CMOS Circuit Design	3	1	0	4
3	PC	MoS Device Physics	3	1	0	4
4	PE-I	Program Elective – I	3	0	0	3
5	PE-II	Program Elective – II	3	0	0	3
6		Digital CMOS Circuit Design Lab	0	1	2	2
7		Analog CMOS Circuit Design Lab	0	1	2	2
8		Seminar-I	0	0	2	1
		TOTAL	**15**	**5**	**6**	**23**

List of Professional Elective Courses in I Semester (Electives – I & II)

S.No.	Course Code	Course Title
1	PE -I	VLSI Technology
2	PE -I	Nano Scale Devices
3	PE -I	MOS Devices Modelling and Characterization
4	PE -I	Digital System Design through HDL
5	PE -II	VLSI Architectures
6	PE -II	Power Management IC Design
7	PE -II	Low Power Design Techniques
8	PE -II	CAD for VLSI

@ Minimum 2/3 themes per elective

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II – Semester

Sl. No.	Course Code	Course Title	L	T	P	C
1	PC	CMOS Mixed Signal Circuit Design	3	1	0	4
2	PC	Physical Design Verification	3	1	0	4
3	PC	VLSI Testing & Testability	3	1	0	4
4	PE-III	Program Elective – III	3	0	0	3
5	PE-IV	Program Elective - IV	3	0	0	3
6		CMOS Mixed Signal Circuit Design Lab	0	1	2	2
7		Physical Design Verification Lab	0	1	2	2
8		Seminar – II	0	0	2	1
		TOTAL	**15**	**5**	**6**	**23**

List of Professional Elective Courses in II Semester (Electives III & IV)

S.No.	Course Code	Course Title
1	PE -III	VLSI signal processing
2	PE -III	MEMS&NEMS
3	PE -III	SoC design
4	PE -III	Fundamentals of Semiconductor Package Manufacturing and Test
5	PE -IV	Advanced VLSI Interconnects
6	PE -IV	Quantum Computing
7	PE -IV	RF IC Design
8	PE -IV	NANO ELECTRONICS

@ Minimum 2/3 themes per elective

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Programme Structure R25 MTech (VLSI, VLSI Design, VLSI System Design, VLSI Micro-Electronic Programme)

III SEMESTER

Sl. No.	Course Code	Course Title	L	T	P	C
1	PC	Research Methodology and IPR / Swayam 12 week MOOC course – RM&IPR	3	0	0	3
2		Summer Internship/ Industrial Training (8-10 weeks)*	-	-	-	3
3		Comprehensive Viva#	-	-	-	2
4		Dissertation Part – A$	-	-	20	10
		TOTAL	**3**	**-**	**20**	**18**

* Student attended during summer / year break and assessment will be done in 3rd Sem.

Comprehensive viva can be conducted courses completed upto second sem.

$ Dissertation – Part A, internal assessment

IV SEMESTER

Sl. No.	Course Code	Course Title	L	T	P	C
1		Dissertation Part – B%	-	-	32	16
		TOTAL	**-**	**-**	**32**	**16**

% External Assessment

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I Semester	**DIGITAL CMOS CIRCUIT DESIGN**	**L**	**T**	**P**	**C**
		3	**1**	**0**	**4**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Analyze MOSFET behavior and CMOS inverter characteristics under static and dynamic conditions.	K4
CO2	Design various combinational and sequential logic blocks using CMOS technology.	K5
CO3	Optimize data path elements such as adders, multipliers, and barrel shifters	K4
CO4	Design and evaluate memory architectures including SRAM and ROM cells	K5
CO5	Interpret and implement circuit layouts using stick diagrams and layout rules	K3

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	H	M	H	H	M	H
CO2	M	M	H	H	M	H
CO3	M	L	M	H	L	H
CO4	M	L	M	M	M	H
CO5	L	H	M	H	M	M

Unit	Syllabus	Contact Hours
Unit I	**MOS Transistor Principles and CMOS Inverter** : MOSFET characteristics under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter – Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay Parameters, Stick Diagram and Layout Diagrams.	12
Unit II	**Combinational Logic Circuits** : Static CMOS Design, Different Styles of Logic Circuits, Logical Effort of Complex Gates, Static and Dynamic Properties of Complex Gates, Interconnect Delay, Dynamic Logic Gates.	12
Unit III	S **Sequential Logic Circuits** : Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Non-Bistable Sequential Circuits.	12
Unit IV	**Arithmetic Building Blocks** : Data Path Circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs.	12
Unit V	**Memory Architectures** : Memory Architectures and Memory Control Circuits: Read-Only Memories, ROM Cells, Read-Write Memories	12

	(RAM), Dynamic Memory Design, 6-Transistor SRAM Cell, Sense Amplifiers.	
	Total	60

TEXT BOOKS:

1. JanRabaey, Anantha Chandrakasan, B Nikolic,"Digital Integrated Circuits: A Design Perspective", Prentice Hall of India, 2nd Edition, Feb 2003
2. N.Weste,K.Eshraghian,"PrinciplesofCMOSVLSIDesign",AddisionWesley,2nd Edition, 1993

REFERENCE BOOKS:

1. MJ Smith,"ApplicationSpecificIntegratedCircuits",AddissonWesley,1997
2. Sung-MoKang &Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill,1998

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I Semester	ANALOG CMOS CIRCUIT DESIGN	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Design basic building blocks of CMOS Analog ICs.	
CO2	Carry out the design of single and two stage operational amplifiers and voltage references	
CO3	Determine the device dimensions of each MOSFETs involved	
CO4	Design various amplifiers like differential, current and operational amplifiers	

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	H	M	H
CO2	M	M	H	H	M	H
CO3	M	L	M	M	L	M
CO4	M	L	H	H	M	H

Unit	Syllabus	Contact Hours
Unit I	MOS Devices and Modeling: The MOS Transistor, Passive Components - Capacitor & Resistor, Integrated Circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.	12
Unit II	Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors - Current Mirror with Beta Helper, Degeneration, Cascode Current Mirror and Wilson Current Mirror, Current and Voltage References, Bandgap Reference.	12
Unit III	Single Stage Amplifier: Common Source Stage with Resistive Load, Diode Connected Load, Triode Load, CS Stage with Source Degeneration, Source Follower, CG Stage, Gain Boosting Techniques, Cascode, Folded Cascode, Choice of Device Models.	12
Unit IV	CMOS Amplifiers and Noise: Inverters, Differential Amplifiers, Cascode Amplifiers. Noise - Statistical Characteristics, Types, Noise in Single-Stage Amplifiers, Noise in Differential Pairs, Noise Bandwidth.	12
Unit V	CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of Op Amps.	12
	Total	60

TEXT BOOKS:

1. CMOS Analog Circuit Design -Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R.G. Meyer, Wiley India, Fifth Edition, 2010.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

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I Semester	**MOS DEVICE PHYSICS**	**L**	**T**	**P**	**C**
		3	**1**	**0**	**4**

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Understand the electrostatics and energy band behavior of MOS structures	K2
CO2	Analyze and model MOSFETs using classical and advanced physical principles	K4
CO3	Evaluate SOI-based MOSFET devices and their operational characteristics	K4
CO4	Apply quantum and ballistic transport concepts to nanoscale transistor design	K3
CO5	Explore and assess modern MOSFET structures including FinFETs and strained-Si devices.	K3

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	H	M	M	M	H	M
CO2	H	M	H	M	H	H
CO3	M	L	H	M	H	M
CO4	H	M	H	M	H	H
CO5	M	M	H	M	H	M

Unit	**Syllabus**	**Contact Hours**
Unit I	MOS Capacitor: Energy Band Diagram of Metal-Oxide-Semiconductor Contacts, Modes of Operation – Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation, CV Characteristics of MOS, LFCV and HFCV, Non-Idealities in MOS – Oxide Fixed Charges, Interfacial Charges, Midgap Gate Electrode, Poly-Silicon Contact, Electrostatics of Non-Uniform Substrate Doping, Ultrathin Gate-Oxide and Inversion Layer Quantization, Quantum Capacitance, MOS Parameter Extraction.	12
Unit II	Physics of MOSFET: Drift-Diffusion Approach for I–V Characteristics, Gradual Channel Approximation, Sub-threshold Current and Slope, Body Effect, Pao & Sah Model, Detailed 2D Effects in MOSFET, High Field and Doping Dependent Mobility Models, High Field Effects and MOSFET Reliability Issues (SILC, TDDB, and NBTI), Leakage Mechanisms in Thin Gate Oxide, High-K Metal Gate MOSFET Devices and Technology Issues, Intrinsic MOSFET Capacitances and	12

	Resistances, Meyer Model.	
Unit III	SOI MOSFET: FDSOI and PDSOI, 1D Electrostatics of FDSOI MOS, VT Definitions, Back Gate Coupling and Body Effect Parameter, I–V Characteristics of FDSOI-FET, FDSOI Sub-threshold Slope, Floating Body Effect, Single Transistor Latch, ZRAM Device, Bulk and SOI FET – Discussions Referring to the ITRS.	12
Unit IV	Nanoscale Transistors: Diffusive, Quasi-Ballistic, and Ballistic Transports, Ballistic Planar and Nanowire FET Modeling – Semi-Classical and Quantum Treatments.	12
Unit V	Advanced MOSFETs: Strain Engineered Channel Materials, Mobility in Strained Materials, Electrostatics of Double Gate and FinFET Devices.	12
	Total	60

TEXT BOOKS:

1. S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, Wiley.
2. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press.
3. M. Lundstrom and J. Guo, *Nanoscale Transistors: Device Physics, Modeling& Simulation*, Springer.

REFERENCE BOOKS:

1. Y. Tsividis, *Operation and Modeling of the MOS Transistor*, Oxford University Press.
2. J. P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, Springer.
3. Selected research papers in relevant and emerging areas.

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I Semester	**VLSI TECHNOLOGY**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	To understand the semiconductor materials, devices and technology historical evaluation	K2
CO2	To analyze the oxidization process and quality measures in the fabrication.	K4
CO3	To explain lithography importance in the semiconductor industry and the various Techniques	K2
CO4	To apply other process steps like etching, implantation and metallization and their applications	K3
CO5	To understand the concepts of electrical testing and packaging of ICs	K2

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	
CO1	M	M	H	M	H	
CO2	M	L	M	L	H	
CO3	M	M	H	L	H	
CO4	M	M	H	M	H	
CO5	L	H	M	L	H	

Unit	**Syllabus**	**Contact Hours**
Unit I	Introduction: Semiconductor materials, semiconductor devices, semiconductor process technology, basic fabrication steps. Crystal Growth: Silicon crystal growth from melt, silicon float-zone process, GaAs crystal growth techniques, material characterization.	12
Unit II	Silicon Oxidation: Thermal oxidation, impurity redistribution during oxidation, masking of silicon dioxide, oxide quality. Photolithography: Optical lithography, E-beam lithography.	12
Unit III	Etching: Wet chemical etching, dry etching. Diffusion: Basic diffusion process, extrinsic diffusion, lateral diffusion.	12
Unit IV	Ion Implantation: Range of implanted ions, implant damage and annealing. Film Deposition: Epitaxial growth techniques, structures and defects in epitaxial layers, dielectric deposition.	12
Unit V	Process Integration: Passive components, bipolar technology, MESFET technology, MEMS technology. IC Manufacturing: Electrical testing, packaging.	12
	Total	60

Text Books:

1. 1. Gary S May & Simon M Sze, Fundamentals of Semiconductor Fabrication, Wiley Student edition,2012

References:

1. S. K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc, 2010.
2. S. M. Sze, VLSI Technology, 2/e, McGraw Hill, 2011.
3. Stephen Cambell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press, 2013.

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I Semester	**NANO SCALE DEVICES**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Describe the physical behavior and scaling trends of long-channel and short-channel MOSFETs	K3
CO2	Understand short-channel effects and propose design solutions using advanced materials	K2
CO3	Analyze 3D transistor structures like FinFETs, DG-ETSOI, and nanowires	K4
CO4	Apply concepts of ballistic and quasi-ballistic transport to nanoscale transistors	K3
CO5	Explore ongoing trends such as NEGF and quantum dots for future nanoelectronics	K2

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	H	L	M	M	H	M
CO2	H	M	M	H	H	H
CO3	H	M	H	H	H	M
CO4	H	M	H	H	H	H
CO5	M	M	H	M	H	M

Unit	**Syllabus**	**Contact Hours**
Unit I	Long Channel MOSFETs: History, Introduction – MOSFET as a Barrier-Controlled Device, MOSFET I–V Characteristics, Drain Current Models, MOSFET Scaling, Subthreshold Characteristics, Substrate Bias and Temperature Dependence, MOSFET Electrostatics – Energy Band Picture, 1D Electrostatic Poisson–Boltzmann Equation, Depletion Approximation, Onset of Inversion, Gate Voltage and Surface Potential, Static and Mobile Charges.	12
Unit II	Short Channel Effects: Charge Sharing, Channel Length Modulation, DIBL, GIDL, Velocity Saturation, MOSFET Breakdown, Concepts of High-K/Metal Gate.	12
Unit III	Advanced Planar and 3D Transistors: FDSOI, DG-ETSOI, FinFETs, Nanowires.	12
Unit IV	Nanoscale Transport: Bottom-Up Approach, Landauer's Formalism, Ballistic and Diffusive Transport – Modes, I–V Characteristics, Conductance, Voltage Drop and Heat Dissipation, Ballistic MOSFET, Ballistic Injection Velocity, Virtual Source Model.	12
Unit V	Current Topics and Open Issues: Strained Silicon Technology, NEGF,	12

	Thermoelectric Effects and Thermoelectric Devices, Quantum Dot Devices – Quantum Capacitance, I–V Characteristics, Self-Consistent Method.	
	Total	60

Text Books:

1. M. Lundstrom, *Fundamentals of Nanotransistors*, World Scientific.
2. T. H. Ning and Y. Taur, *Fundamentals of Modern VLSI Devices*, Pearson Education India Pvt. Ltd.

References:

1. D. A. Neamen, *Semiconductor Physics and Devices*, McGraw-Hill Higher Education.
2. S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, Wiley.

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I Semester	**MOS DEVICES MODELLING AND CHARACTERIZATION**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Understand and derive the electrostatic and CV behavior of MOS capacitors.	K2
CO2	Analyze threshold voltage variations and bias effects in MOS devices.	K4
CO3	Evaluate MOSFET operation across different regions and environmental conditions.	K3
CO4	Apply small-signal models including Ebers-Moll and charge control for AC analysis.	K3
CO5	Study and model short-channel effects in modern deep-submicron devices	K2

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	H	M	M	H	M	M
CO2	H	M	M	H	H	H
CO3	M	M	H	M	M	H
CO4	M	M	H	M	M	H
CO5	H	M	H	H	H	H

Unit	**Syllabus**	**Contact Hours**
Unit I	Basic Concepts: Energy Band Diagram of Metal-Oxide-Semiconductor Contacts, Modes of Operation – Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation.	12
Unit II	Bias Conditions: CV Characteristics of MOS, LFCV and HFCV, Non-Idealities in MOS – Oxide Fixed Charges, Interfacial Charges, Threshold Voltage Capacitance-Voltage Relation, The Three-Terminal MOS Structure, Effect of Body Bias on Surface Conditions, Threshold Voltage with Body Bias.	12
Unit III	MOSFETs: The Four-Terminal Metal-Oxide-Semiconductor Transistor, Strong Inversion, Moderate Inversion and Weak Inversion Current, Voltage Models, Effective Mobility, Effect of Source and Drain Series Resistance, Temperature Effects, Breakdown.	12
Unit IV	Small Signal Models: Ebers-Moll Model, Charge Control Model, Small-Signal Models for Low and High Frequency, Switching Characteristics.	12
Unit V	Short Channel Effects: Short Channel and Thin Oxide Effects, Carrier Velocity Saturation, Channel Length Modulation, Charge Sharing,	12

	Drain Induced Barrier Lowering (DIBL), Punch Through, Hot Carrier Effects, Impact Ionization, Velocity Overshoot, Ballistic Operation, Quantum Mechanical Effects, DC Gate Current, Junction Leakage, Band-to-Band Tunneling, Gate Induced Drain Leakage (GIDL), MOSFET Scaling.	
	Total	60

Text Books:

1. S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed., Wiley Eastern, 1981.
2. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 2013.

References:

1. Y. Tsividis and C. McAndrew, *The MOS Transistor*, 3rd ed., Oxford University Press, 2013.
2. Y. P. Tsividis, *Operation and Modelling of the MOS Transistor*, McGraw-Hill, 1987.
3. E. Takeda, *Hot-Carrier Effects in MOS Transistors*, Academic Press, 1995.

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I Semester	**DIGITAL SYSTEM DESIGN THROUGH HDL**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	**Design and simulate digital systems using VHDL and Verilog in behavioral, dataflow, and structural styles**	K5
CO2	**Implement combinational and sequential logic components in HDL**	K4
CO3	**Translate logic circuits into synthesizable HDL code using FSMs and control logic**	K3
CO4	**Use synthesis tools and interpret synthesized netlists for implementation**	K2
CO5	**Evaluate and test digital systems for faults using CAD tools and test methodologies**	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	H	H	H	H	M	H
CO2	M	M	H	H	M	H
CO3	M	M	H	H	M	H
CO4	M	H	M	M	M	M
CO5	M	M	H	H	M	H

Unit	**Syllabus**	**Contact Hours**
Unit I	Digital Logic Design using VHDL: Introduction, designing with VHDL, design entry methods, logic synthesis, entities, architecture, packages and configurations, types of models: dataflow, behavioral, structural, signals vs. variables, generics, data types, concurrent vs. sequential statements, loops and program controls. Digital Logic Design using Verilog HDL: Introduction, Verilog data types and operators, binary data manipulation, combinational and sequential logic design, structural models of combinational logic, logic simulation, design verification and test methodology, propagation delay, truth table models using Verilog.	12
Unit II	Combinational Logic Circuit Design using VHDL: Combinational circuits building blocks: multiplexers, decoders, encoders, code converters, arithmetic comparison circuits, VHDL for combinational circuits, adders - half adder, full adder, ripple-carry adder, carry look-ahead adder, subtraction, multiplication.	12

	Sequential Logic Circuit Design using VHDL: Flip-flops, registers & counters, synchronous sequential circuits: basic design steps, Mealy state model, design of FSM using CAD tools, serial adder example, state minimization, design of counter using sequential circuit approach.	
Unit III	Digital Logic Circuit Design Examples using Verilog HDL: Behavioral modeling, data types, Boolean-equation-based behavioral models of combinational logics, propagation delay and continuous assignments, latches and level-sensitive circuits in Verilog, cyclic behavioral models of flip-flops and latches and edge detection, comparison of styles for behavioral model; behavioral model, multiplexers, encoders and decoders, counters, shift registers, register files, dataflow models of a linear feedback shift register, machines with multi cycle operations, ASM and ASMD charts for behavioral modeling, design examples, keypad scanner and encoder.	12
Unit IV	Synthesis of Digital Logic Circuit Design: Introduction to synthesis, synthesis of combinational logic, synthesis of sequential logic with latches and flip-flops, synthesis of explicit and implicit state machines, registers and counters.	12
Unit V	Testing of Digital Logic Circuits and CAD Tools: Testing of logic circuits, fault model, complexity of a test set, path-sensitization, circuits with tree structure, random tests, testing of sequential circuits, built-in self test, printed circuit boards, computer aided design tools, synthesis, physical design.	12
	Total	60

TEXT BOOKS:

1. Stephen Brown & Zvonko Vranesic, “Fundamentals of Digital logic design with VHDL”, Tata McGraw Hill,2nd edition.
2. Michael D. Ciletti, “Advanced digital design with the Verilog HDL”, Eastern economy edition, PHI.

REFERENCE BOOKS:

1. Stephen Brown & Zvonko Vranesic, “Fundamentals of Digital logic with Verilog design”, Tata McGraw Hill,2nd edition.
2. Bhaskar, “VHDL Primer”,3rd Edition, PHI Publications.
3. Ian Grout, “Digital systems design with FPGAs and CPLDs”, Elsevier Publications.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

I Semester	**VLSI ARCHITECTURES**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Design RISC architecture and control units for a given instruction set.	K5
CO2	Improve the performance of RISC processors by applying pipelining techniques	K4
CO3	Translate DSP algorithms into efficient hardware architectures and design associated building blocks	K3
CO4	Analyze the impact of retiming, unfolding, and folding on the performance of DSP architectures	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	M	M	H	H	H	M
CO2	M	M	H	H	H	M
CO3	H	M	H	H	H	H
CO4	M	M	H	M	H	M

Unit	**Syllabus**	**Contact Hours**
Unit I	Instruction Set Architectures and CPU Performance: Overview of Instruction Set Architectures – CISC, RISC, and DSP Processors, CPU Performance and Its Factors, Evaluating Performance Metrics.	12
Unit II	Design of RISC Processor: Designing the Datapath and Control Unit for a RISC Processor, Multicycle Implementation of RISC Architecture.	12
Unit III	Enhancing Performance with Pipelining: Overview of Pipelining, Pipelined Datapath, Pipelined Control Unit, Pipeline Hazards – Data, Control, and Structural Hazards, Techniques for Hazard-Free Pipelined RISC Implementation.	12
Unit IV	Multiprocessors and DSP Algorithm Representation: Introduction to Multiprocessors, Multiprocessors Connected by a Single Bus and Network, Network Topologies, Evolution vs. Revolution in Computer Architecture, DSP Algorithm Representation – Data Flow Graphs, Loop Bound and Iteration Bound, Algorithms for Computing Iteration Bound.	12
Unit V	Pipelining, Parallel Processing, and VLSI Performance Techniques: Introduction to Pipelining and Parallel Processing, FIR Filter Pipelining, Parallel Processing Techniques, Pipelining and Parallel Processing for Low Power, VLSI Architecture Optimization Techniques – Retiming, Unfolding, and Folding.	12
	Total	60

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

TEXT BOOKS:

1. D.A,Patterson And J.L.Hennessy, Computer Organization and Design: Hardware/ Software Interface, Elsevier, 2011, 4th Edition
2. Keshab Parhi, VLSI digital signal processing systems design and Implementations, Wiley 1999
3. NPTEL Courses (https://nptel.ac.in/courses/108105157)

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

I Semester	**POWER MANAGEMENT IC DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Understand the need for power management circuits in modern VLSI systems.	K2
CO2	Identify and explain various components of a power management system, with emphasis on DC-DC converters	K4
CO3	Design chip-level DC-DC converters based on given system-level specifications	K5
CO4	Apply a top-down design methodology to implement efficient DC-DC converter topologies	K3

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	M	L	H	M	H	H
CO2	M	M	H	M	H	M
CO3	H	M	H	M	M	H
CO4	H	H	H	H	M	H

Unit	**Syllabus**	**Contact Hours**
Unit I	Introduction to Power Management and Voltage Regulation: Introduction to power management and voltage regulators, need of power management, power management applications, classification of power management, power delivery of a VLSI system, power conversion, discrete vs. integrated power management, types of voltage regulators (switching vs. linear regulators) and applications, converter's performance parameters (voltage accuracy, power conversion efficiency, load regulation, line regulation, line and load transient response, settling time, voltage tracking), local vs. remote feedback, Kelvin sensing, Point-of-Load (POL) regulators.	12
Unit II	Principles of Linear Voltage Regulators: Linear regulators, Low Drop-Out Regulator (LDO), source and sink regulators, shunt regulator, pass transistor, error amplifier, small signal and stability analysis, compensation techniques, current limiting, power supply rejection ratio (PSRR), NMOS vs. PMOS regulator, current regulator.	12
Unit III	Switching DC-DC Converters: Design and Control Technique: Switching DC-DC converters and control techniques, types (buck, boost, buck-boost), power FETs, choosing L and C, PWM modulation (leading, trailing and dual edge modulation), losses in switching converters, output ripple, voltage vs. current mode control, CCM and DCM modes, small signal model of DC-DC converter, loop gain	12

	analysis of uncompensated DC-DC converter, type-I, type-II and type-III compensation, compensation of voltage mode and current mode DC-DC converters, hysteretic control, switched capacitor DC-DC converters.	
Unit IV	Systematic Design of DC-DC Converters: Top-down design approach of a DC-DC converter, selecting topology, switching frequency and external components, sizing power FETs, segmented power FET, designing gate driver, PWM modulator, error amplifier, oscillator, ramp generator, feedback resistors, current sensing, PFM/PSM mode for light load, effect of parasitic on reliability and performance, current limit and short circuit protection, soft start control, chip level layout and placement guidelines, board level layout guidelines, EMI considerations.	12
Unit V	Emerging Technologies in Power Management: Introduction to advanced topics in power management, digitally controlled DC-DC converters, digitally controlled LDOs, adaptive compensation, dynamic voltage scaling (DVS), Single-Inductor Multiple-Outputs (SIMO) converters, DC-DC converters for LED lighting, Li-ion battery charging circuits.	12
	Total	60

TEXT BOOKS:

1. Switch-mode Power Supplies: SPICE Simulations and Practical Designs, Christophe P Basso, BPB Publications, 2010.
2. PowerManagementTechniquesforIntegratedCircuitDesignByKe-HorngChen,Wiley-Blackwell, 2016.

REFERENCE BOOKS:

1. Fundamentals of Power Electronics, 2nd edition by Robert W.Erickson, Dragan Maksimovic, Springer (India) Pvt. Ltd, 2005.
2. Bernhard Wicht, Design of Power Management Integrate Circuits, Wiley, 2024.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

I Semester	**LOW POWER DESIGN TECHNIQUES**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Understand the sources of power dissipation in CMOS circuits and estimation techniques	K2
CO2	Apply probabilistic and circuit-level techniques for low-power logic design.	K3
CO3	Design power-efficient architectures using switching activity reduction and voltage scaling.	K5
CO4	Analyze and reduce power consumption in clock distribution networks	K4
CO5	Apply algorithmic and architectural techniques for system-level power optimization.	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	H	M	H	M	H	H
CO2	M	L	M	M	H	H
CO3	M	L	H	H	H	H
CO4	M	M	H	H	H	H
CO5	M	M	H	H	H	M

Unit	**Syllabus**	**Contact Hours**
Unit I	Introduction to Low Power Design: Need for low power VLSI chips, sources of power dissipation, device and technology impact on low power, impact of technology scaling, technology and device innovation, power estimation, SPICE circuit simulators, gate-level logic simulation, capacitive power estimation, static power, gate-level capacitance estimation, architecture-level analysis, Monte-Carlo simulation.	12
Unit II	Probabilistic Power Analysis and Circuit-Level, Logic-Level Design: Random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy, low power design, power consumption in circuits, flip-flop and latch design, high capacitance nodes, low power digital cell libraries, gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.	12
Unit III	Low Power Architecture and Systems: Power and performance management, switching activity reduction, parallel architectures with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.	12

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Unit IV	Low Power Clock Distribution: Power dissipation in clock distribution, single driver vs. distributed buffers, zero skew vs. tolerable skew, chip and package co-design techniques for clock networks.	12
Unit V	Algorithm and Architectural Level Methodologies: Introduction, design flow, algorithmic level analysis and optimization, architectural level estimation and synthesis.	12
	Total	60

Text Books:

1. K. Roy and S. Prasad, *Low-Power CMOS VLSI Circuit Design*, Wiley, 2000.
2. G. K. Yeap, *Practical Low Power Digital VLSI Design*, Kluwer Academic Publishers (KAP), 2002.
3. J. M. Rabaey and M. Pedram (Eds.), *Low Power Design Methodologies*, Kluwer Academic Publishers, 1997

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

I Semester	**CAD FOR VLSI**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	**Understand the VLSI design flow and the stages of physical design automation**	K2
CO2	**Apply algorithms for partitioning, floor planning, pin assignment, and placement**	K3
CO3	**Analyze and implement routing algorithms for global and detailed routing**	K4
CO4	**Explore physical design techniques for FPGAs and MCMs**	K3
CO5	**Design robust I/O circuits and understand ESD, latch-up prevention, and clock distribution challenges**	K5

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	M	M	H	H	H	M
CO2	M	M	H	H	H	M
CO3	M	M	H	H	H	M
CO4	M	L	H	H	H	M

Unit	**Syllabus**	**Contact Hours**
Unit I	VLSI Physical Design Automation: VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.	12
Unit II	Partitioning, Floor Planning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing. Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint-based floor planning, Rectangular Dualization. Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel pin assignments. Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.	12
Unit III	Global Routing and Detailed Routing: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms. Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.	12

Unit IV	Physical Design Automation of FPGAs and MCMs: FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model. Introduction to MCM Technologies, MCM Physical Design Cycle.	12
Unit V	Chip Input and Output Circuits: ESD Protection, Input Circuits, Output Circuits and L(di/dt) noise, On-chip clock Generation and Distribution, Latch-up and its prevention.	12
	Total	60

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

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M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

I Semester	**ANALOG CMOS CIRCUIT DESIGN LAB**	**L**	**T**	**P**	**C**
		0	**1**	**2**	**2**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools	K3
CO2	Grasp the significance of various cmos analog circuits in full-custom IC Design flow	K4
CO3	Have the ability to explain the Physical Verification in Layout Design	K3
CO4	Fully Appreciate the design and analyze of analog and mixed signal simulation	K4
CO5	Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation	K5

List of Experiments:

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. simple current mirror
6. cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

Lab Requirements:
Software:
Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator/ Industry Equivalent Standard Software
Hardware:
Personal Computer with necessary peripherals, configuration and operating System.

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I Semester	**DIGITAL CMOS CIRCUIT DESIGN LAB**	**L**	**T**	**P**	**C**
		0	**1**	**2**	**2**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools	K3
CO2	Grasp the significance of various design logic Circuits in full-custom IC Design.	K4
CO3	Have the ability to explain the Physical Verification in Layout Extraction	K3
CO4	Fully Appreciate the design and analyze of CMOS Digital Circuits	K4
CO5	Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation	K5

#Based on suggested Revised BTL

List of Experiments:

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software:

Industry Standard Software (Mentor Graphics Tool/Cadence/ Synopsys/Equivalent)

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

II Semester	**CMOS MIXED SIGNAL CIRCUIT DESIGN**	**L**	**T**	**P**	**C**
		3	**1**	**0**	**4**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Understand the necessity of mixed signal systems	K2
CO2	Analyze Op-Amp to meet the mixed signal specifications	K4
CO3	Design CMOS comparators to meet the high-speed requirements of digital circuitry	K5
CO4	Develop efficient data converter circuits for mixed signal systems	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	M	M	H
CO2	L	L	M	H	M	H
CO3	M	M	M	H	H	H
CO4	M	L	M	H	H	H

Unit	**Syllabus**	**Contact Hours**
UNIT - I	Two-Stage OP-AMP Design :Parasitic Effects on Design of Two-Stage OP-AMP, Wide-Swing Cascode Current Mirrors, Design of Rugged Biasing Circuit with Temperature-Independent Compensation, Challenges in Mixed-Signal Circuit Design. Switched Capacitor Circuits : Constituents: Op-Amp, Capacitors, Switches, Non-overlapping Clocks; Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator, Parasitic-Insensitive Integrators, Signal-Flow-Graph Analysis, Design of Filters Based on Switched Capacitor Circuits.	12
UNIT - I	Sample-and-Hold Circuit: Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Charge-Injection Errors, Making Charge-Injection Signal Independent, Minimizing Errors Due to Charge-Injection, Effect of Offset and Application of Switched Capacitor Circuits to Minimize Offset Errors, Parasitic Effects.	12
UNIT - III	Comparators: Ideal Comparator, Practical Model of Comparator, Resolving Capability, Propagation Delay, Small Signal Analysis, Conditions for Slewing, Evaluation of Propagation Delay for Single Pole and Two Pole Comparators, Design of Linear Response Comparators, Slew-Rate Limited Comparators, Comparators with Positive Feedback, Analysis of Latched Comparators, Architecture of	12

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	High-Speed Comparators, Self-Biased Comparators, Push Pull Comparators.	
UNIT - IV	Data Converters : Classification, Ideal D/A Converter, Ideal A/D Converter, Quantization Noise: Deterministic and Stochastic Approach, Signed Codes, Performance Limitations: Resolution, Offset and Gain Error, Accuracy and Linearity, Integrating Converters, Design of Successive-Approximation Converters, DAC-Based and Charge-Redistribution SAR, Interleaved, Pipelined, Flash, Principles of Sigma-Delta ADC, Testing of Data Converters.	12
UNIT - V	PLL and Oscillators : Basic PLL Architecture, VCO, Divider, Phase Detector, Loop Filter, PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model, Limitations, PLL Characterization and Design Example, Jitter and Phase Noise: Period Jitter, Cycle Jitter, Adjacent Period Jitter, Spectral Representations and PDF of Jitter, Ring and LC Oscillators, Phase Noise in Oscillators and PLLs.	12
	Total	60

TEXT BOOKS:

1. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2012, 2nd Edition.
2. Behzad Razavi, Design of Analog CMOS Integrated Circuits"McGraw Hill Education, 2017, 2nd Edition.
3. R.JacobBaker,CMOS:Mixed-SignalCircuitDesign,Wiley,2008,2nd Edition.

REFERENCE BOOKS:

1. Roubik Gregorian and Gabor C. Temes, Analog MOS integrated circuits for signal processing, Wiley, 1986.
2. Roubik Gregorian, Introduction to CMOS Op-Amps and Comparators, Wiley, 2008.
3. RuiPauloda Silva Martins and Pui-InMak,"Analog and Mixed-Signal Circuits in Nano scale CMOS", Springer, 2024.

Other Suggested Readings:

- NPTELCourses(https://onlinecourses.nptel.ac.in/noc22_ee34/preview)

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II Semester	**PHYSICAL DESIGN VERIFICATION**	**L**	**T**	**P**	**C**
		3	**1**	**0**	**4**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Understand the relationship between design automation algorithms and Various constraints posed by VLSI fabrication and design technology	K2
CO2	Adapt the design algorithms to meet the critical design parameters.	K3
CO3	Identify layout optimization techniques and map them to the algorithms	K3
CO4	Develop proto-type EDA tool and test its efficacy	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	H	H	M
CO2	L	M	M	H	M	M
CO3	M	M	M	H	H	L
CO4	H	M	H	H	M	M

Unit	**Syllabus**	**Contact Hours**
UNIT I	VLSI Design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication. Design styles: Full Custom, Standard Cell, Gate Arrays, Field Programmable Gate Arrays, Sea of Gates and Comparison, System Packaging Styles, Multi-Chip Modules. Design Rules, Layout of Basic Devices, Fabrication Process and Its Impact on Physical Design, Interconnect Delay, Noise and Crosstalk, Yield and Fabrication Cost.	12
UNIT II	Factors, Complexity Issues and NP-hard Problems. Basic Algorithms (Graph and Computational Geometry): Graph Search Algorithms, Spanning Tree Algorithms, Shortest Path Algorithms, Matching Algorithms, Min-Cut and Max-Cut Algorithms, Steiner Tree Algorithms.	12
UNIT III	Basic Data Structures: Atomic Operations for Layout Editors, Linked List of Blocks, Bin Based Methods, Neighbour Pointers, Corner Stitching, Multi-Layer Operations.	12
UNIT IV	Graph Algorithms for Physical Design: Classes of Graphs, Graphs Related to a Set of Lines, Graphs Related to a Set of Rectangles, Graph Problems in Physical Design, Maximum Clique and Minimum Coloring, Maximum k-Independent Set Algorithm, Algorithms for Circle Graphs.	12

UNIT V	Partitioning Algorithms: Design Style Specific Partitioning Problems, Group Migrated Algorithms, Simulated Annealing and Evolution. Floor Planning and Pin Assignment, Routing and Placement Algorithms.	12
	Total	60

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008

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II Semester	**VLSI TESTING & TESTABILITY**	**L**	**T**	**P**	**C**
		3	**1**	**0**	**4**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Identify the significance of testable design	K3
CO2	Understand the concept of yield and identify the parameters influencing the same	K2
CO3	Specify fabrication defects, errors, and faults	K3
CO4	Implement combinational and sequential circuit test generation algorithms	K4
CO5	Identify techniques to improve fault coverage	K5

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	L	L	M	H	M	L
CO2	M	M	M	H	H	M
CO3	M	L	M	H	H	M
CO4	M	M	M	H	M	H
CO5	M	L	M	H	H	M

Unit	**Syllabus**	**Contact Hours**
UNIT I	Role of Testing in VLSI Design Flow, Testing at Different Levels of Abstraction, Fault, Error, Defect, Diagnosis, Yield. Types of Testing, Rule of Ten, Defects in VLSI Chip. Modelling Basic Concepts, Functional Modelling at Logic Level and Register Level, Structure Models, Logic Simulation, Delay Models. Various Types of Faults, Fault Equivalence and Fault Dominance in Combinational and Sequential Circuits.	12
UNIT II	Fault Simulation Applications, General Fault Simulation Algorithms: Serial and Parallel, Deductive Fault Simulation Algorithms.	12
UNIT III	Combinational Circuit Test Generation, Structural Vs Functional Test, ATPG, Path Sensitization Methods. Difference Between Combinational and Sequential Circuit Testing, Five and Eight Valued Algebra, Scan Chain-Based Testing Method.	12
UNIT IV	D-Algorithm Procedure, Problems. PODEM Algorithm, Problems on PODEM Algorithm. FAN Algorithm, Problems on FAN Algorithm. Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-Hoc Design, Generic Scan-Based Design.	12

UNIT V	Classical Scan-Based Design, System Level DFT Approaches. Test Pattern Generation for BIST, Circular BIST, BIST Architectures. Testable Memory Design: Test Algorithms, Test Generation for Embedded RAMs.	12
	Total	60

TEXT BOOKS:

1. M. Abramovici, M. Breuer, and A. Friedman, “Digital Systems Testing and Testable Design, IEEE Press, 1990.
2. M. Bushnell and V. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2000.

REFERENCE BOOKS:

1. Stroud,“A Designer’s Guide to Built-in Self-Test”, Kluwer AcademicPublishers,2002
2. V.Agrawal and S.C.Seth, Test Generation for VLSI Chips, Computer Society Press. 1989

Other Suggested Readings:

1. NPTELCourses(https://archive.nptel.ac.in/courses/117/105/117105137/)

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M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

II Semester	**VLSI SIGNAL PROCESSING**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Understand the fundamentals of DSP systems, data flow modeling, and techniques like pipelining and parallel processing for FIR filters	K2
CO2	Apply retiming, unfolding, and algorithmic strength reduction techniques to optimize DSP architectures	K3
CO3	Analyze and implement pipelined and parallel processing architectures for IIR filters and fast convolution methods	K4
CO4	Design and evaluate bit-level arithmetic structures such as multipliers, FIR filters, and distributed arithmetic implementations	K5
CO5	Explore synchronous, wave, and asynchronous pipelining techniques and apply numerical strength reduction methods in DSP systems	K3

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	L	L	M	M	H	H
CO2	M	L	M	H	H	H
CO3	M	L	M	H	H	H
CO4	M	L	M	H	M	H
CO5	M	L	M	M	M	H

Unit	**Syllabus**	**Contact Hours**
UNIT I	Introduction to DSP: Typical DSP Algorithms, Benefits of DSP Algorithms, Representation of DSP Algorithms. Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques.	12
UNIT II	Folding: Introduction, Folding Transform, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems. Unfolding: Introduction, Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming, Applications of Unfolding.	12
UNIT III	Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for	12

	Space Representations Containing Delays.	
UNIT IV	Fast Convolution: Introduction, Cook-Toom Algorithm, Winograd Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.	12
UNIT V	Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction Techniques, Power Estimation Approaches. Programmable DSP: Evaluation of Programmable DSPs, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.	12
	Total	60

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

II Semester	**MEMS & NEMS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Understand the principles and processes involved in micro-fabrication techniques used for MEMS structures	K2
CO2	Analyze material behavior under mechanical stress and apply elasticity theory to MEMS structures like beams, cantilevers, and plates	K4
CO3	Model and evaluate MEMS capacitive switches and actuators, including electromechanical behavior, damping, and reliability aspects	K3
CO4	Design and assess MEMS-based thermal sensors and explore challenges in Bio-MEMS applications	K5
CO5	Understand and evaluate the design and operation of optical MEMS devices such as 2-D and 3-D switches	K2

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	H	H	H
CO2	M	L	M	H	M	H
CO3	M	L	M	H	M	H
CO4	H	L	H	H	M	M
CO5	M	L	M	M	H	M

Unit	Syllabus	Contact Hours
UNIT I	Introduction to Micro-Fabrication: Cleaning, Oxidation, Diffusion, Mask Making, Lithography, Etching, Ion Implantation, Chemical Vapor Deposition (CVD), Physical Vapor Deposition (PVD), Metallization. Surface Micromachining and Bulk Micromachining, Deep Reactive Ion Etching (DRIE), LIGA Process, Fabrication of High Aspect Ratio Deformable Structures.	12
UNIT II	Elasticity in Materials: Stress and Strain Calculations, Normal and Shear Strains, Constitutive Relations, Plane Stress, Biaxial Stress, Residual Stress, Energy Relations. Load-Deflection Calculations in Beams and Cantilevers (Rectangular Cross Section), Elastic Deformation in Square Plates, Resonant Frequency Calculations using Rayleigh-Ritz Method.	12
UNIT III	MEMS Capacitive Switch and Actuators: Lumped Model of MEMS Capacitive Switch, Pull-in Voltage, Electromechanical Deflection Modelling, Pull-in Instability, Switching Time and Pull-in Voltage	12

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

	Scaling, Physical Effects in Nanoscale Gap-Size, Squeeze-Film Damping, Perforated MEMS Capacitive Switch. Comb Actuators, Accelerometer, Pressure Sensor. Energy Approach: Lagrangian Mechanics Applied to MEMS Capacitive Switches. Reliability Issues in RF MEMS Capacitive Switches.	
UNIT IV	MEMS Sensors: Thermal Sensors, Interaction of Thermal-Electrical Fields, Numerical Design of Thermal Sensors. Introduction to Bio-MEMS and Associated Design Challenges.	12
UNIT V	Optical MEMS: 2-D and 3-D Optical MEMS Switches, Design Examples and Case Studies.	12
	Total	60

REFERENCE BOOKS:

1. Rebeiz, G.M., *RF MEMS: Theory Design and Technology*, Wiley
2. Stephen D. Senturia, *Microsystem Design*, Kluwer Academic
3. Madou, M., *Fundamentals of Microfabrication*, CRC Press
4. Sandana A., *Engineering Biosensors: Kinetics and Design Applications*, Academic Press

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

II Semester	**SOC DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Understand and estimate key design metrics and requirements including area, latency, throughput, energy, and power	K2
CO2	Implement both hardware and software solutions, formulate hardware/software trade-offs, and perform hardware/software co-design	K4
CO3	Analyze issues in system-on-chip design associated with interconnection structures, performance, and power consumption	K4
CO4	Use System C programming and high-level synthesis (HLS) for design and modeling	K2
CO5	Design and optimize a modern System-on-a-Chip	K5

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	L	M	H	H	H	H
CO2	M	M	H	H	H	H
CO3	M	M	H	H	H	M
CO4	M	H	H	H	H	M
CO5	H	H	H	H	H	M

Unit	**Syllabus**	**Contact Hours**
UNIT I	SoC Design Approach: Basics of Chips and SoC ICs, SoC Design: SoC CPU/IP Cores, Co-processor, Cache, DRAM Controller, SoC Synthesis, Static Timing Analysis (STA), Design for Testability, Verification, Physical Design.	12
UNIT II	Hardware-Software Co-Synthesis: Partitioning, Cycle Time, Die Area and Cost, Power, Area-Time-Power Trade-offs and Chip Reliability, Real-Time Scheduling, Hardware Acceleration.	12
UNIT III	Virtual Prototyping and High-Level Synthesis (HLS): Mapping High-Level Language Applications to Hardware, Transaction-Level Modeling and Electronic System-Level Languages, Hardware Accelerators, Media Instructions, Coprocessors, System-Level Design Methodology, High-Level Synthesis (C-to-RTL), Hardware Synthesis and Architecture	12

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M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

	Techniques, Source-Level Optimizations.	
UNIT IV	SoC Interconnection Structures: Bus-Based Interconnection, Bus Protocols: AMBA AXI Bus, AXI4-Stream, IBM Core Connect, Avalon. Interconnection Structures, Network on Chip (NoC) Interconnection and NoC Systems, IP Interfacing.	12
UNIT V	Performance/Power Analysis of SoCs: System-Level Modeling and Integration, Simulation Platform for Performance Analysis of SoC/MPSoC, Use Cases and Examples.	12
	Total	60

Books Recommended

1. Veena Chakravarthi, *A Practical Approach to VLSI System on Chip (SoC) Design – A Comprehensive Guide*, Springer, 2020
2. S. Pasricha and N. Dutt, *On-Chip Communication Architectures: System on Chip Interconnect*, Morgan Kaufmann–Elsevier Publishers, 2008
3. Keating, M., *The Simple Art of SoC Design*, Springer, 2011

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

II Semester	**FUNDAMENTALS OF SEMICONDUCTOR PACKAGE MANUFACTURING AND TEST**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Understand the evolution of semiconductor packaging technologies and explain the various backend assembly processes involved in IC packaging.	K2
CO2	Analyze the selection and role of substrate materials, interconnect technologies, and encapsulation methods, along with reliability challenges like delamination and thermal cycling.	K4
CO3	Demonstrate knowledge of electrical and mechanical test techniques at both wafer and package levels, including DC/AC testing, BIST, JTAG, and mechanical integrity tests.	K5
CO4	Apply reliability concepts, failure analysis techniques, and quality control methodologies to assess and improve package manufacturing outcomes.	K4
CO5	Evaluate advanced and emerging semiconductor packaging trends such as 3D stacking, TSVs, RF/MEMS packaging, and environmentally sustainable practices through industry case studies.	K5

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	H	H	L
CO2	M	M	M	H	H	M
CO3	M	M	M	H	H	M
CO4	H	M	M	H	H	M
CO5	H	M	H	M	H	M

Unit	**Syllabus**	**Contact Hours**
UNIT I	Overview of Semiconductor Packaging and Assembly: Semiconductor Packaging Evolution and Types (e.g., BGA, LGA, Flip Chip). Backend Assembly Processes: Wafer Dicing, Die Attach, Wire Bonding, Flip-Chip Bonding, Encapsulation/Molding, Marking.	12
UNIT	Package Substrate and Interconnect Technology: Substrate Materials	12

II	and Package Interconnections, Role of Glues, Underfill, and Encapsulants. Introduction to Package Interconnect Reliability (Delamination, Thermal Cycling).	
UNIT III	Electrical and Mechanical Testing of Packages: Wafer-Level Test, Package-Level Test, Final IC Test. Test Equipment Overview: DC, AC, Functional Tests. Built-In Self-Test (BIST), JTAG Boundary Scan, and Burn-In Testing. Mechanical Tests: Shear, Bend, Pull Strength.	12
UNIT IV	Reliability, Failure Analysis, and Quality Control: Reliability Fundamentals: Bathtub Curve, Failure Mechanisms, Failure Rate Modeling. Process Control Systems for Package Manufacturing Quality. Failure Analysis: Visual Inspection, Decapsulation, X-ray, Electrical Test Correlation.	12
UNIT V	Industry Case Studies & Emerging Packaging Trends: 3D-Stacked Packages, Multi Die Integration, High Density Interposers. Packaging for RF, MEMS, and Sensor Applications. Emerging Materials and Processes: Micro Bump, Through Silicon Vias (TSV), Advanced Substrates. Environmental and Sustainability Considerations in Packaging.	12
	Total	60

Books Recommended

1. Veena Chakravarthi, *A Practical Approach to VLSI System on Chip (SoC) Design – A Comprehensive Guide*, Springer, 2020.
2. S. Pasricha and N. Dutt, *On-Chip Communication Architectures: System on Chip Interconnect*, Morgan Kaufmann–Elsevier Publishers, 2008.
3. Michael Keating, *The Simple Art of SoC Design*, Springer, 2011.
4. Patrick Schaumont, *A Practical Introduction to Hardware/Software Co-design*, Springer, 2009.
5. François Ghenassia, *Transaction-Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems*, Springer, 2010.
6. Wolfgang Grotker, Shuqing Liao, Grant Martin, and Stuart Swan, *System Design with SystemC*, Springer, 2002.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

II Semester	**ADVANCED VLSI INTERCONNECTS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Gain insight into transmission line parameters of VLSI interconnects.	K3
CO2	Understand novel and emerging solutions for future VLSI interconnect technologies.	K2
CO3	Analyze the impact of inductive effects in high-speed interconnects.	K4
CO4	Examine the influence of quantum effects in nanoscale interconnects.	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	M	H	H
CO2	M	L	M	H	H	H
CO3	M	L	M	H	H	H
CO4	M	L	M	H	H	H

Unit	Syllabus	Contact Hours
UNIT I	Introduction: Introduction to VLSI Interconnects, The Distributed RC Interconnect Model, Elmore Delay in Interconnects, Scaling Effects in Interconnects, Simulation and Delay Mitigation in RC Interconnects.	12
UNIT II	Inductive Effects: Inductive Effects in Interconnects, Distributed RLC Interconnect Model, Transmission Line Equations, When to Consider the Inductive Effects?, Equivalent Elmore Model for RLC Interconnects, Two-Pole Model of RLC Interconnects from ABCD Parameters, RLC Interconnect Simulation.	12
UNIT III	Skin Effect and Electromigration: Origin of the Skin Effect, Effective Resistance at High Frequencies, Power Dissipation due to Interconnects, Electromigration in Interconnects, Mitigation of Electromigration.	12
UNIT IV	Crosstalk: Capacitive Coupling in Interconnects, Crosstalk Effects in Two Identical Interconnects, Mitigation Techniques, Analysis and Simulation of Coupled Interconnects. Extraction of Capacitance, Extraction of Inductance, Estimation of Interconnect Parameters from S-parameters.	12
UNIT V	Quantum Effects: Quantum Conductance, Quantum Capacitance, Kinetic Inductance, Graphene Nanoribbon Interconnects, Analysis and Simulation of Interconnect Considering Quantum Effects.	12
	Total	60

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

Text Books:

1. Ashok K.Goel, High-Speed VLSI Interconnects,2007.
2. . Y.S. Diamand, Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications, 2009.

Reference Books:

1.H.S Philip Wong and Deji Akinwande,Carbon nanotube and Graphene Device Physics,2011.

Other Suggested Readings:

NPTELCourses(https://onlinecourses.nptel.ac.in/noc22_ee125/preview

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M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

II Semester	**QUANTUM COMPUTING**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Understand the fundamental principles of quantum computation and the concept of qubits.	K2
CO2	Analyze multi-qubit systems and quantum communication protocols.	K4
CO3	Analyze multi-qubit systems and quantum communication protocols.	K4
CO4	Design and implement basic quantum algorithms and quantum circuits.	K5
CO5		

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	M	M	M
CO2	M	L	M	M	M	M
CO3	M	L	M	M	M	M
CO4	M	L	M	M	M	M

Unit	**Syllabus**	**Contact Hours**
UNIT I	Review of Quantum Mechanics and Motivation for Quantum Computation. Qubit: The Qubit State - Matrix and Bloch Sphere Representation - Computational Basis - Unitary Evolution.	12
UNIT II	Multi-Qubit States: No-Cloning Theorem, Superdense Coding, Pure States to Bell States, Bell Inequalities. Protocols with Multi-Qubits: Swapping, Teleportation. Gates: CNOT, Toffoli Gate, NAND, FANOUT, Walsh-Hadamard.	12
UNIT III	Measurement: Projective Operators - General, Projective and POVM Measurement. Ensemble: Density Operators - Pure and Mixed Ensemble - Time Evolution - Post Measurement Density Operator. Composite Systems: Partial Trace, Reduced Density Operator, Schmidt Decomposition, Purification, Bipartite Entanglement.	12
UNIT IV	Quantum Computing: Classical Computing Using Qubits, Quantum Parallelism, Deutsch's Algorithm, Deutsch-Jozsa Algorithm.	12
UNIT V	Quantum Circuits: Basic Gates, ABC Decomposition, Gray Codes, Universal Gates, Principle of Deferred and Implicit Measurements. Quantum Fourier Transform and Applications: Phase Estimation, Order	12

	Finding, Factoring, Discrete Logarithm, Hidden Subgroup Problems. Role of Prime Factoring in Classical Cryptography. Search Algorithms, Quantum Error Correcting Codes, Physical Realization of Qubits.	
	Total	60

Text Books:

1. M.A.Nielsen and I.L.Chuang, Quantum Computation and Quantum Information, Cambridge University Press, 2010, 10th Anniversary Edition
2. Chris Bernhardt, Quantum Computing for Everyone, The MITPress,2019.
3. RayLaPierre, Introduction to Quantum Computing,Springer,2021.

Reference Books:

1. Quantum Theory: Concepts and Methods, AsherPeres, Kluwer Academic Publishers,1993.
2. Venkateswaran Kasirajan, Fundamentals of Quantum Computing: Theory and Practice, Springer, 2021.

Other Suggested Readings:

1. NPTELCourses(https://nptel.ac.in/courses/106106232

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M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

II Semester	**RF IC DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Understand the key design bottlenecks and challenges specific to RF integrated circuit design.	K2
CO2	Identify various noise sources and develop appropriate noise models for RF devices and systems.	K4
CO3	Evaluate and compare different transmitter and receiver architectures used in RF systems.	K4
CO4	Design and analyze various RF amplifier topologies for communication applications.	K5
CO5		

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	M	H	H
CO2	M	L	M	M	H	H
CO3	M	L	M	M	H	H
CO4	M	L	M	M	H	H

Unit	**Syllabus**	**Contact Hours**
UNIT I	Basic Concepts of RFIC Design: Design Bottlenecks of RFIC Design, Non-linearity and Time Invariance, Sensitivity and Dynamic Range, Passive Impedance Transformation. RF Radio Receiver Front End Non-Idealities and Design Parameters: Effects of Nonlinearity, 1 dB Compression Point, Derivation of Required Noise Figure at Receiver Front End, Required IIP3 at Receiver Front End, Partitioning of Required NF at Receiver Front End and IIP3 into Individual NF and IIP3.	12
UNIT II	Noise: Noise Sources in MOSFETs, Modeling of Thermal Noise and Flicker Noise, Noise in Analog Integrated Circuits.	12
UNIT III	Transceiver Architectures: General Considerations, Receiver Architecture, Transmitter Architecture, Transceiver Performance Tests.	12
UNIT IV	Low Noise Amplifier (LNA): Introduction, General Philosophy, Matching Networks, Comparison of Narrowband and Wideband LNA. Wideband LNA Design: DC Bias, Gain and Frequency Response, Noise Figure. Narrowband LNA: Principles, Core	12

	Amplifier Design, Noise Figure, Power Dissipation, Trade-offs between Noise Figure and Power Dissipation, Noise Contribution from Other Sources.	
UNIT V	Mixers and Frequency Synthesizers: Mixers: Active Mixer, Modeling Mixers, Unbalanced Mixer Circuits, Single Balanced Mixer Circuit, Double Balanced Mixer Circuits, Quantitative Description of Gilbert Mixer, Conversion Gain, Distortion, Analysis of Gilbert Mixer. Passive Mixers: Switching Mixer, Distortion in Unbalanced Switching Mixer, Conversion Gain and Noise. Frequency Synthesizer: PLL Based Frequency Synthesizer: Concepts of PLL, Phase Detector, Charge Pump, RF Synthesizer Architectures, Frequency Dividers, VCO, LC Oscillators, Ring Oscillator, Phase Noise, Loop Filter and System Design.	12
	Total	60

Text Books:

1. Bosco Leung,VLSI for wireless communication, Springer, 2011, 2nd Edition. Behad Razavi, RF Micro electronics, Prentice Hall,2011,2nd Edition.

Reference Books:

1. Rovert Caverly, CMOS RFIC Design Principles, Artech House,1stEdition,2007
2. Hooman Darabi, Radio Frequency Integrated Circuits and Systems, Cambridge University Press, 2020, 2ndEdition.

Other Suggested Readings:

1. NPTEL Courses (https://nptel.ac.in/courses/106103182/)

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

II Semester	**NANO ELECTRONICS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	To understand the basic science behind the design and fabrication of nano scale systems	K2
CO2	To understand and formulate new engineering solutions for current problems and competing technologies for future applications	K2
CO3	To be able make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development	K3
CO4	To gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems	K4
CO5		

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	M	H	H
CO2	M	L	M	M	H	H
CO3	M	L	M	M	H	H
CO4	M	L	M	M	H	H

Unit	**Syllabus**	**Contact Hours**
UNIT I	Overview: Nano devices, Nano materials, Nano device characterization, Definition of Technology node, MOS capacitor, MOS Scaling theory, Moore’s Law and Koomey's law.	12
UNIT II	Issues in scaling MOS transistors: Short channel effects, Description of a typical 65 nm CMOS technology, Role of interface quality and related process techniques, Gate oxide thickness, scaling trend, SiO2 vs High-k gate dielectrics, Integration issues of high-k, Interface states, bulk charge, band offset, stability, reliability - Qbd high field, possible candidates, CV and IV techniques, Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot. Metal gate transistor: Motivation, requirements, Integration Issues.	12
UNIT III	Non-classical MOS transistor: Requirements and Novel devices - SOI: PD-SOI and FD-SOI, Ultra-thin body SOI, Double gate transistors, integration issues. Vertical transistors - FinFET and	12

	Cylindrical gate FET.	
UNIT IV	Novel devices: Tunnel FET, Negative-Capacitance (NC) FET. Metal source/drain junctions - Properties of Schottky junctions on Silicon, Germanium and compound semiconductors - Work function pinning.	12
UNIT V	Emerging Nano MOSFETs: Strain, quantization, Advantages of Germanium over Silicon, PMOS versus NMOS. Compound semiconductors MOSFETs in the context of channel quantization and strain, Heterostructure MOSFETs, exploiting novel materials, strain, quantization. CNT, Graphene, Nanotubes, Nanorods and other nano-structures.	12
	Total	60

Text Books:

1. Kenneth J. Klabunde and Ryan M. Richards, “Nanoscale Materials in Chemistry”, 2nd edition,John Wiley and Sons, 2009.
2. I Gusev and A ARempel, “Nanocrystalline Materials”, Cambridge International Science
   Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
3. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, James Murday, “Nanoscience and Nanotechnology”, Tata McGraw Hill Education 2012.

Reference Books:

1. Bharat Bhushan, “Springer Handbook of Nanotechnology”, Springer, 3rd edition, 2010.
2. Kamal K. Kar, “Carbon Nanotubes: Synthesis, Characterization and Applications”, Research Publishing Services; 1 st edition, 2011, ISBN-13: 978-9810863975.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

II Semester	**CMOS MIXED SIGNAL CIRCUIT DESIGN LAB**	**L**	**T**	**P**	**C**
		0	**1**	**2**	**2**

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Implement discrete-time signal processing circuits tailored for mixed-signal system requirements	K4
CO2	Apply layout methodologies and design techniques specific to mixed-signal integrated circuits to ensure signal integrity and performance	K3
CO3	Design operational amplifiers optimized for operation in mixed-signal environments with appropriate gain, bandwidth, and stability	K5
CO4	Design high-speed comparators with enhanced resolution and low latency for time-critical mixed-signal application	K5
CO5	Develop data converters and RF circuits considering performance trade-offs in mixed-signal design scenarios.	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

Cycle	**Syllabus**	
Cycle 1	1) Fully compensated op-amp with resistor and Miller compensation 2) Comparator design: a. Linear Response b. Slew-rate limited	
Cycle 2	3) Switched capacitor circuits: i. Parasitic sensitive integrator ii. Parasitic insensitive integrator iii. Delay free integrators iv. Low Pass filter 4) Data converters (ADC, DAC for given specifications) 5) Layouts and parasitic extraction	

Text Books:

1. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2012, 2nd Edition.
2. Roubik Gregorian and Gabor C.Temes, Analog MOS integrated circuits for signal processing, Wiley, 1986.

Reference Books:

1. Roubik Gregorian, Introduction to CMOS Op-Amp and Comparators, Wiley,1999.
2.Alan Hastings, Theart of Analog Layout, Wiley, 2005

Other Suggested Readings:

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M.**TECH R25 VLSI & ALLIED COURSE STRUCTURE AND SYLLABUS**

II Semester	**PHYSICAL DESIGN VERIFICATION LAB**	**L**	**T**	**P**	**C**
		0	**1**	**2**	**2**

1. NPTELCourses(https://onlinecourses.nptel.ac.in/noc23_ee142/preview)

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Implement and analyze graph-based algorithms used in physical design automation, including depth-first search, breadth-first search, spanning trees, and shortest path algorithms	K4
CO2	Apply computational geometry techniques such as line sweep and extended line sweep methods in geometric problem-solving relevant to VLSI layout	K3
CO3	Design and evaluate partitioning algorithms including Kernighan–Lin, Fiduccia–Mattheyses, and Goldberg–Burstein algorithms, as well as simulated annealing and evolution-based approaches	K5
CO4	Implement floorplanning techniques using constraint-based, integer programming, hierarchical tree, rectangular dualization, and simulated evolution strategies	K4
CO5	Develop and compare routing algorithms for two-terminal and multi-terminal nets, including maze routing and Steiner tree-based algorithms like SMST and Z-RST	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

Cycle	**Syllabus**	
Cycle 1	1) Graph algorithms: a) Graph search algorithms: i. Depth first search ii. Breadth first search b) Spanning tree algorithm: i. Kruskal's algorithm c) Shortest path algorithm: i. Dijkstra algorithm ii. Floyd-Warshall algorithm d) Steiner tree algorithm	
Cycle 2	2) Partitioning algorithms: a. Kernighan–Lin algorithm b. Fiduccias–Mattheyses algorithm c. Simulated annealing and evolution algorithms 3) Floor planning algorithms: i) Constraint based methods ii) Integer programming based methods	

	iii) Rectangular dualization based methods iv) Simulated evolution algorithms 4) Routing algorithms - Two terminal algorithms: a) Maze routing algorithms: i) Lee's algorithm ii) Soukup's algorithm iii) Hadlock algorithm b) Line-Probe algorithm c) Shortest path based algorithm	

Software required: C/C++ Programming Language /Relevant software

Reading:

1) Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic,1998.

2) Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.